Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **BALANCE**
2. **IN –**
3. **IN +**
4. **V –**
5. **BALANCE**
6. **OUTPUT**
7. **V +**

**.058”**

**.058”**

**MASK**

**REF**

**N**

**S**

**C**

**9**

**9**

**1**

**5**

**1**

**Z**

**2 1 7**

**3 4 5 6**

**NOTE: Chip back should be connected to V- (or leave floating)**

**Top Material: Al**

**Backside Material: Si or Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V- or leave Floating**

**Mask Ref: NSC99151Z**

**APPROVED BY: DK DIE SIZE .058” X .058” DATE: 7/11/16**

**MFG: NATIONAL THICKNESS .015” P/N: LF411**

**DG 10.1.2**

#### Rev B, 7/19/02